TRANSMITTAL FORM

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Total Number of Pages in This Submission	20

Application No.	09/823,070
Filing Date	March 30, 2001
First Named Inventor	Priya Rajagopal
Art Unit	2154
Examiner Name	Nguyen, D.
Attorney Docket Number	42390P10458

ENCLOSURES ***(check all that apply)***

- [x] Fee Transmittal Form
  - Fee Attached
- [ ] Amendment / Response
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
  - [ ] PTO/SB/08
- [ ] Certified Copy of Priority Document(s)
- [ ] Response to Missing Parts/ Incomplete Application
  - [ ] Basic Filing Fee
  - [ ] Declaration/POA
- [ ] Response to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
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- [ ] After Allowance Communication to TC
- [ ] Appeal Communication to Board of Appeals and Interferences
- [x] Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- [ ] Proprietary Information
- [ ] Status Letter
- [x] Other Enclosure(s) *(please identify below):*

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Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Gordon R. Lindeen III, Reg. No. 33,192 BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Signature	
Date	June 6, 2006

CERTIFICATE OF MAILING/TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop Appeal Brief-Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Typed or printed name	**Debbie Casias**		
Signature	Debbie Casias	Date	**June 6, 2006**

Based on PTO/SB/21 (09-04) as modified by Blakely, Sokoloff, Taylor & Zafman (wlr) 11/30/2005.
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FEE TRANSMITTAL for FY 2005

Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27.

TOTAL AMOUNT OF PAYMENT	($)	500.00

Complete if Known	
Application Number	09/823,070
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METHOD OF PAYMENT *(check all that apply)*

☐ Check ☐ Credit card ☐ Money Order ☐ None ☐ Other (please identify): _____

☒ Deposit Account Deposit Account Number: 02-2666 Deposit Account Name: Blakely, Sokoloff, Taylor & Zafman LLP

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FEE CALCULATION

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet.	
2053	130	2053	130	Non-English specification	
1251	120	2251	60	Extension for reply within first month	
1252	450	2252	225	Extension for reply within second month	
1253	1,020	2253	510	Extension for reply within third month	
1254	1,590	2254	795	Extension for reply within fourth month	
1255	2,160	2255	1,080	Extension for reply within fifth month	
1401	500	2401	250	Notice of Appeal	
1402	500	2402	250	Filing a brief in support of an appeal	500.00
1403	1,000	2403	500	Request for oral hearing	
1451	1,510	2451	1,510	Petition to institute a public use proceeding	
1460	130	2460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
1809	790	1809	395	Filing a submission after final rejection (37 CFR § 1.129(a))	
1810	790	2810	395	For each additional invention to be examined (37 CFR § 1.129(b))	

Other fee (specify) _____

SUBTOTAL (2) ($) 500.00

SUBMITTED BY Complete (if applicable)

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Signature				Date	06/06/06

Based on PTO/SB/17 (12-04) as modified by Blakely, Sokoloff, Taylor & Zafman (wlr) 12/15/2004.
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Docket No.: 42390P10458 Patent

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re the Patent Application of:		
	Williams, C.	
Serial No.:	09/183,732	Art Unit: 2611
Filed:	October 30, 1998	Examiner: Koenig, A.
For:	Method and Apparatus for Surfing Through Multiple Sources Based on User-Definable Preferences	

Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313

IN SUPPORT OF APPELLANT'S APPEAL
TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

Sir:

Applicant (hereafter "Appellant") hereby submits this Brief in triplicate in support of its appeal from a final decision by the Examiner, mailed January 9, 2006 in the above-captioned case. Appellant respectfully requests consideration of this appeal by the Board of Patent Appeals and Interferences for allowance of the above-captioned patent application.

An oral hearing is not desired.

TABLE OF CONTENTS

I. REAL PARTY IN INTEREST

The invention is assigned to Intel Corporation of 2200 Mission College Boulevard, Santa Clara, California 95052-8119.

II. RELATED APPEALS AND INTERFERENCES

To the best of Appellant's knowledge, there are no appeals or interferences that are related to, will directly affect, will be directly affected by, or have a bearing on the Board's decision in the present appeal.

III. STATUS OF THE CLAIMS

Claims 1-20 are currently pending in the above-referenced application. No claims have been allowed. All pending claims were rejected in the Final Office Action mailed January 9, 2006, and are the subject of this appeal.

All pending claims stand rejected under 35 U.S.C. § 103. Several claims stand rejected as indefinite under 35 U.S.C. § 112.

IV. STATUS OF AMENDMENTS

In response to the Final Office Action mailed on January 9, 2006, rejecting claims 1-20, Appellant timely filed a Notice of Appeal on April 10, 2006.

A copy of all claims on appeal is attached hereto as Appendix A.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

The present invention allows two separate processing engines, such as microprocessors, for example in two networked computers or in a parallel processing system, to be synchronized with a very high accuracy. The invention can be applied to a variety of systems for a variety of different benefits as discussed above and has a minimal impact on network traffic loads. In one embodiment, the synchronization is applied to microprocessors based on the tick counter of each respective processor. The tick count counter value is maintained in a register of a typical microprocessor and is updated at the speed of the microprocessor. The value can be read from the register with a standard, simple, assembly language instruction. As a result, the value provides very high accuracy commensurate with the processor speed and can be obtained very quickly. For an Intel Pentium ® II processor that runs at 233MHz, synchronization can be obtained with an accuracy on the order of a few nanoseconds. For an Intel Pentium ® 4 processor that runs at 1.5GHz, synchronization can be obtained with an accuracy on the order of half a nanosecond.. *See Detailed Description, paragraph 12.*

The arguments of this brief are presented in the context only of Claim 1, however, examples of components of the other independent claims as shown in the drawings are pointed out for the Board's convenience. Turning to the first independent claim, Claim 1 presents a method that comprises:

includes obtaining a processor tick counter value from a first processing engine (*See Figure 1, 16, 18, Figure 4, 402, Figure 2, 34, 46*);

comparing the obtained processor tick counter value to a processor tick counter value from a second processing engine (*See Figure 1, 12, Figure 4, 402, Figure 2, 54-58*);

determining a timing offset using the comparison (*See Figure 2, 54*); and

sending the timing offset to the first processing engine to apply to the execution of instructions by the first processing engine which are normalized to the timing of the second processing engine (*See Figure 2, 60, 62*).

Claim 9 is a Beauregard claim based on Claim 1.

Claim 14 is an apparatus claim directed to a synchronized computing network. The elements of Claim 14 include:

a first processing engine (*See Figure 1, 16, 18*) having a processor tick counter;

a second processing engine (*See Figure 1, 12)* having a processor tick counter;

a communications link (*See Figure 5, 425*) to send a value from the processor tick counter of the first processing engine to the second processing engine at one time;

a processor (*See Figure 5, 402*) of the second processing engine to compare the processor tick counter value from the first processing engine to a processor tick counter value from the second processing engine, to determine a timing offset using the comparison, and to apply the timing offset to the execution of instructions by the first processing engine which are normalized to the timing of the second processing engine.

The remaining claims are dependent on one of the claims mentioned above.

The invention allows instructions to be executed in a distributed processing environment with much closer synchronization than with other approaches..

VI. GROUNDS OF REJECTION

A. Claims 34, 5, 11, 12, 16, and 17 stand rejected as indefinite. This rejection is not under appeal.

B. Claims 1-20 stand rejected as obvious over under 35 U.S.C. § 103(a) over Kubo et al., U.S. Patent No. 6,832,326 ("Kubo") in view of Grimwood, U.S. Patent No. 6,243,369 ("Grimwood").

No claims were indicated as allowable.

VII. ARGUMENT

This argument is directed against the second ground of rejection identified at Section VI.B. (obviousness). It would appear that the first ground of rejection may be traversed by replacing "the" with "a" in the rejected claims. The first ground of rejection is not appealed.

The rejections of the other claims are not discussed here in the interests of brevity. The claims not discussed herein are believed to be allowable on the above grounds as well as for the additional recitations expressly set forth in each such claim respectively.

A. THE OBVIOUSNESS REJECTION IS IN ERROR BECAUSE NEITHER REFERENCE TEACHES SENDING A TIMING OFFSET TO ANOTHER PROCESSOR NOR APPLYING SUCH AN OFFSET TO THE EXECUTION OF INSTRUCTIONS AS SPECIFICALLY RECITED IN THE CLAIMS

Kubo shows clock synchronization. As stated in the abstract, the timer value of each processor is adjusted with the measured propagation delay time. Grimwood shows a cable TV system (1:20) in which frequency (or clock rate 8:52) is synchronized and frames are aligned (13:23) for transmissions of video and customer purchase data through coaxial cable.

With respect to Kubo, the Examiner correctly acknowledges with respect to e.g. Claim 1, that Kubo does not teach or suggest the last two elements of determining and sending. The Examiner suggests that Grimwood discloses these two elements.

> The two elements are set forth below for the Board's convenience:
> "determining a timing offset using the comparison; and
> "sending the timing offset to the first processing engine to apply to the execution of instructions by the first processing engine which are normalized to the timing of the second processing engine."

As to determining a timing offset, Grimwood's timing offset has nothing to do with processor tick counter values. (In brief, Grimwood does not suggest any use of a

timing offset for tick counter values.) The section cited by the Examiner is related to determining a timebase conversion factor (22:42) . The clock ticks referred to in Grimwood are frame counter clock ticks (21:60) and timestamp counter clock ticks (22:3) or timesample clock ticks (22:11). The timebase conversion factor is used to recover upstream data (22:54). So, Grimwood has a timebase conversion factor based on frame counter clocks. Grimwood does not have a timing offset and nothing like the comparison of Claim 1, between processor tick counter values. Accordingly, the cited section does nothing to suggest a timing offset such as that of the present invention.

As to sending the timing offset, this claim element further recites "to apply to operations which are normalized to the timing of the second processing engine." Applicants have carefully reviewed the cited section in Column 3 (Summary of the Invention) as well as Claim 6. In Column 3, the RU synchronizes its clock to the CU. It then transmits upstream data to the CU and the CU receives it using its own CU clock due to the synchronization. There is no timing offset being sent and there are no operations that are normalized to any timing. The clocks are simply synchronized.

In Claim 6, the remote node modem independently arranges its transmission to coincide with the clock frequency, superframe counter and minislot counter of the headend. There is no sending of timing offsets. Further, the sending of data is not normalized to the timing of the second processing engine (the sender). To the contrary, the upstream data is transmitted based on the clock and counter values of the headend (recipient).

Even if "apply to operations" in Claim 1 were construed to mean "demodulated and demultiplexed" (3:9), Grimwood teaches away from the present invention. In Grimwood, the RU receives downstream data, calculates its timespace conversion and frame counter offsets, and adapts its upstream transmissions to the master clock of the CU (headend). The benefit is that the CU can receive the transmission using its own CU clock (3:12 the "suitable phase and amplitude adjustments" are conventional training

techniques). In the present invention, the first engine sends its tick counter value to the second engine and then uses an offset provided by the second engine to apply to operations.

The distinction from Grimwood is very clear in the claimed recitation that the timing offset is applied to the execution of instructions.

Summarizing using the example of Claim 1, Claim 1 is believed to be allowable because:

Neither reference suggests comparing tick counter values;

Neither reference suggests determining offsets for tick counter values. (In Kubo, the tick value is written over with the received tick value.);

Neither reference suggests sending a timing offset from one component to another. (In Grimwood, the determined frame offset, frequency corrections etc. are used by the modem that determines them.);

Neither reference suggests applying a timing offset to the execution of instructions.

Given these significant failings in the cited references, Applicants respectfully submit that the present application is allowable.

B. THE OBVIOUSNESS REJECTION IS IN ERROR BECAUSE THE TICK COUNTER IN GRIMWOOD IS NOT A PROCESSOR TICK COUNTER

Grimwood does not suggest performing operations using processor tick counter values. The first mention of any tick counter does not occur until Column 47, line 58. This is not a processor tick counter but a master clock tick counter in both the CU and RU. There is no description of this clock tick counter. It would appear to be used only to generate an offset signal 415 to the symbol counter 422 of Figure 13 that is used to determine minislot, frame, and superframe boundaries (Col. 41, lines 35 et seq.). The

boundary information can be used for reception and also to ensure that uplink transmissions arrive at the CU at the proper time (Col. 41, line 52).

C. THE OBVIOUSNESS REJECTION IS IN ERROR BECAUSE GRIMWOOD'S CABLE TV SYNCRONIZATION SCHEME IS NOT IN THE SAME FIELD AS SYNCHRONIZING INSTRUCTION EXECUTION AS RECITED IN THE CLAIMS

Grimwood is not within the scope of the prior art that would be considered by a person of average skill in the art of the present application. Grimwood is about establishing a reference frame and kiloframe boundary time for sending uplink SCDMA packets, so that all of the sending RU's will be synchronized together and with the receiving CU. This ensures that the uplink packets are sent at the right time (see e.g. Column 14, lines 61 to Column 15, line 21, not definition of offset at Col. 14, line 65.).

Grimwood refers to ranging as the process of determining an offset 415 between the CU and RU timing. Ranging is a process of determining the difference between CU and RU. Traditionally, using the distance, the propagation delay can be determined and using the propagation delay, the timing of a transmission can be advanced to compensate for the propagation delay (time it will take the transmission to reach the receiver).

Grimwood accomplishes the ranging not by measuring a physical distance but by sending a sample of the CU timestamp counter at regular intervals (Column 16, lines 8 et seq.)

On the other hand, Claim 1, for example refers to executing instructions by one processor synchronized to the timing of another processor. As explained above,

Grimwood does not teach or suggest this. Grimwood synchronizes data transmission between multiple transmitters and receivers.

D. SUMMARY

Grimwood would require significant modification to be adapted into a combination with Kubo to achieve the present invention. The modifications would at least include using changing the CU and RU to processors, using processor tick counter registers instead of clock counters, determining the offset at the CU and then sending the offset to the RU, instead of the opposite approach used in Grimwood, and then using the offset for instruction execution instead of for SCDMA data communication.

Applicants respectfully submit that such a modification of Grimwood to use with Kubo simply goes too far beyond the disclosure of either reference. There is nothing in Grimwood to suggest that the techniques may be applied to the art of Kubo and the necessary modifications take Grimwood completely away from any solution or application that may have been contemplated in the reference.

VIII. CONCLUSION

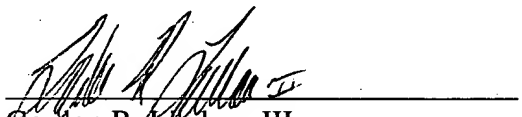
Appellant respectfully submits that all the appealed claims in this application are patentable and requests that the Board of Patent Appeals and Interferences overrule the Examiner and direct allowance of the rejected claims.

This brief is submitted in triplicate, along with a check for $500.00 to cover the appeal fee for one other than a small entity as specified in 37 C.F.R. § 1.17(c). Please charge any shortages and credit any overpayment to out Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Date: June 6, 2006



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APPENDIX OF CLAIMS (37 C.F.R. § 1.192(c)(7))

1. A method comprising:

obtaining a processor tick counter value from a first processing engine;

comparing the obtained processor tick counter value to a processor tick counter value from a second processing engine;

determining a timing offset using the comparison; and

sending the timing offset to the first processing engine to apply to the execution of instructions by the first processing engine which are normalized to the timing of the second processing engine.

2. The method of Claim 1, wherein obtaining a processor tick counter value comprises sending a request message from the second processing engine to the first processing engine, and receiving a reply from the first processing engine at the second processing engine.

3. The method of Claim 2, wherein the processor tick counter value at the second processing engine is determined by recording the time at which the request message is sent.

4. The method of Claim 2, wherein the processor tick counter value at the second processing engine is determined by recording the time at which the reply is received.

5. (Original) The method of Claim 2 further comprising repeating sending a request message, recording the time, receiving a reply, recording the time and determining a timing offset until the determined timing offsets are within a predetermined variability range.

6. (Original) The method of Claim 1 further comprising applying a time stamp to a message sent from the second processor, the time stamp being determined by applying the determined timing offset.

7. (Original) The method of Claim 1 further comprising receiving an instruction having an execution time and interpreting the execution time by applying the determined timing offset.

8. (Original) The method of Claim 1, further comprising:

obtaining a processor frequency from the first processing engine;

obtaining a processor frequency from the second processing engine; and

correcting the timing offset for any difference between the first processing engine frequency and the second processing engine frequency.

9. (Previously Presented) A machine-readable medium having stored thereon data representing sequences of instructions which, when executed by a machine, cause the machine to perform operations comprising:

obtaining a processor tick counter value from a first processing engine;

comparing the obtained processor tick counter value to a processor tick counter value from a second processing engine;

determining a timing offset using the comparison; and

sending the timing offset to the first processing engine to apply to the execution of instructions by the first processing engine ~~operations~~ which are normalized to the timing of the second processing engine.

10. (Previously Presented) The machine-readable medium of Claim 9, wherein the instructions for obtaining a processor tick counter value comprise further instructions which, when executed by the machine, cause the machine to perform further operations comprising sending a request message from the second processing engine to the first processing engine, and receiving a reply from the first processing engine at the second processing engine.

11. (Previously Presented) The machine-readable medium of Claim 10, further comprising instructions which, when executed by the machine, cause the machine to perform further operations comprising determining the processor tick counter value at the second processing engine by recording the time at which the request message is sent.

12. (Previously Presented) The machine-readable medium of Claim 10, further comprising instructions which, when executed by the machine, cause the machine to perform further operations comprising determining the processor tick counter value at the second processing engine by recording the time at which the reply is received.

13. (Previously Presented) The machine-readable medium of Claim 9, further comprising instructions which, when executed by the machine, cause the machine to perform further operations comprising:

obtaining a processor frequency from the first processing engine;

obtaining a processor frequency from the second processing engine; and

correcting the timing offset for any difference between the first processing engine frequency and the second processing engine frequency.

14. (Previously Presented) A synchronized computing network comprising:

a first processing engine having a processor tick counter;

a second processing engine having a processor tick counter;

a communications link to send a value from the processor tick counter of the first processing engine to the second processing engine at one time;

a processor of the second processing engine to compare the processor tick counter value from the first processing engine to a processor tick counter value from the second processing engine, to determine a timing offset using the comparison, and to apply the timing offset to the execution of instructions by the first processing engine which are normalized to the timing of the second processing engine.

15. (Previously Presented) The synchronized computing network of Claim 14, wherein the first processor sends the processor tick counter value as a reply to a request message from the second processing engine.

16. (Previously Presented) The synchronized computing network of Claim 15, wherein the processor tick counter value at the second processing engine is determined by recording the time at which the request message is sent.

17. (Previously Presented) The synchronized computing network of Claim 15, wherein the processor tick counter value at the second processing engine is determined by recording the time at which the reply is received.

18. (Previously Presented) The synchronized computing network of Claim 14, wherein the first processing engine and the second processing engine run at different frequencies and wherein the processor corrects the timing offset for the difference between the first processing engine frequency and the second processing engine frequency.

19. (Previously Presented) The synchronized computing network of Claim 14, wherein the processor of the second processing engine applies a time stamp to a message sent from the second processing engine, the time stamp being determined by applying the determined timing offset.

20. (Previously Presented) The synchronized computing network of Claim 14, wherein the processor of the second processing engine executes an instruction at a time based on the determined timing offset.

XI. EVIDENCE APPENDIX

None.

XII. RELATED PROCEEDINGS APPENDIX

None.